REMARKS

This paper is responsive to an Office action dated January 11, 2006. Claims 1-66 were examined. Claims 1-51 and 53-58 stand rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 5,362,996 to Yizraeli. Claims 52 and 59-66 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Specification

The specification is amended to correct typographical errors.

Claim Rejections Under 35 USC §102

Claims 1-51 and 53-58 stand rejected under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 5,362,996 to Yizraeli. Claim 1 is amended to clarify the invention and to correct grammatical errors. Regarding amended claim 1, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> `sensing simultaneous transitions of a first signal and a second adjacent signal,`

as required by claim 1. The Office action relies on sensing circuit 15 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, the sensing circuit 15 of Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest sensing simultaneous transition of a first signal and a second

adjacent signal, as required by claim 1. Accordingly, Applicants respectfully request that the rejection of claim 1 be withdrawn.

Regarding claim 11, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> delaying switching of a first signal in the event a second signal transitions at the same time as the first signal,

as required by claim 11. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest delaying switching of a first signal in the event that a second signal transitions at the same time as the first signal, as required by claim 11. Accordingly, Applicants respectfully request that the rejection of claim 11 be withdrawn.

Claim 16 is amended to clarify the invention and to correct grammatical errors. Regarding amended claim 16, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> a device configured to sense simultaneous transitions of a first signal and a second adjacent signal,

as required by amended claim 16. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, Yizraeli teaches senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest delaying switching of the first signal in the event the second signal transitions at the same time as the first signal, as required by claim 16. Accordingly, Applicants respectfully request that the rejection of claim 16 be withdrawn.

Claim 17 is amended to clarify the invention and to correct grammatical errors. Regarding amended claim 17, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> `sense simultaneous transitions of a first signal and a second adjacent signal`

as required by claim 17. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, the sensing circuit 15 of Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest sensing simultaneous transitions of a first signal and a second adjacent signal, as required by claim 17. Accordingly, Applicants respectfully request that the rejection of claim 17 be withdrawn.

Regarding claim 22, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> a second device configured to sense simultaneous transitions of the first signal and the third signal,

as required by claim 22. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, the sensing circuit 15 of Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest sensing simultaneous transitions of the first signal and the third signal, as required by claim 22. Accordingly, Applicants respectfully request that the rejection of claim 22 be withdrawn.

Regarding claim 26, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> delay switching of a first signal in the event a second adjacent signal transitions at the same time as the first signal,

as required by claim 26. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, Yizraeli teaches sensing whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest delaying switching of a first signal in the event a second adjacent signal transitions at the same time as the first signal, as required by claim 26. Accordingly, Applicants respectfully request that the rejection of claim 26 be withdrawn.

Regarding claim 27, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> a first device configured to delay switching of a first signal in the event a second adjacent signal transitions at the same time as the first signal,

as required by claim 27. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, Yizraeli teaches senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest a first device configured to delay switching of a first signal in the event a second adjacent signal transitions at the same time as the first signal, as required by claim 27. Accordingly, Applicants respectfully request that the rejection of claim 27 be withdrawn.

Claim 31 is amended to clarify the invention and to correct grammatical errors. Regarding amended claim 31, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> means for sensing simultaneous transitions of a first signal and a second adjacent signal

as required by claim 31. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, the sensing circuit 15 of Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest means for sensing a simultaneous transition of the first signal and

the second signal, as required by claim 31. Accordingly, Applicants respectfully request that the rejection of claim 31 be withdrawn.

Regarding claim 41, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> means for delaying switching of a first signal in the event a second adjacent signal transitions at the same time as the first signal,

as required by claim 41. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, Yizraeli teaches sensing whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest means for delaying switching of a first signal in the event a second adjacent signal transitions at the same time as the first signal, as required by claim 41. Accordingly, Applicants respectfully request that the rejection of claim 41 be withdrawn.

Regarding claim 46, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> a circuit configured to detect a transition of a first signal and a transition of a second signal and provide a delay signal when the transitions of the first and the second signals occur simultaneously,

as required by claim 46. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, the sensing circuit 15 of Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest a circuit configured to detect a transition of a first signal and a transition of a second signal and provide a delay signal when the transitions of the first and the second signals occur simultaneously, as required by claim 46. Accordingly, Applicants respectfully request that the rejection of claim 46 be withdrawn.

Regarding claim 54, Applicants respectfully maintain that Yizraeli, alone or in combination with other references of record fails to teach or suggest

> a circuit configured to detect a transition of each signal of a plurality of signals and provide a delay signal when any adjacent signals simultaneously transition,

as required by claim 54. The Office action relies on sensing circuit 15 and delay circuits 30-37 and 60-67 of FIG. 1 of Yizraeli to supply this teaching. Yizraeli teaches that "[w]hen a delay is to be added to the data signal line, a high input is provided from the sensing circuit 15 to the data delay circuit 70 on delay enable signal line 14." Col. 4, lines 39-41. Yizraeli teaches further that

> [i]f a pad 13, is bonded to V_{CC} the sensing circuit 30 [sensing circuit 15] provides a 'high' signal on delay enable signal line 14. The high signal enables each of the delay circuits 30-37 and 60-67 thereby implementing the staggered mode. If the integrated circuit implementing the present invention, is to be utilized in a

> package having multiple power pairs the staggering function can be disabled by not coupling the sensing circuit 15 to Vcc.

Col. 6, lines 49-57. Accordingly, the sensing circuit 15 of Yizraeli senses whether or not a staggered mode is enabled based on a voltage level received by a pad coupled to the sensing circuit and enables the delay circuits based on whether the staggered mode is enabled. Nowhere does Yizraeli teach or suggest a circuit configured to detect a transition of each signal of a plurality of signals and provide a delay signal when any adjacent signals simultaneously transition, as required by claim 54. Accordingly, Applicants respectfully request that the rejection of claim 54 be withdrawn.

Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter in claims 52, and 59-66. Applicants believe that claims 52, and 59-66 depend from allowable claims and are allowable for at least this reason.

Additional Remarks

Claim 6 is amended to clarify the invention.

Claim 21 is amended to clarify the invention.

Claim 22 is amended to clarify the invention.

Claim 25 is amended to correct grammatical errors.

Claim 31 is amended to clarify the invention.

Claim 41 is amended to correct a grammatical error.

Claim 44 is amended to correct grammatical errors.

In summary, claims 1-66 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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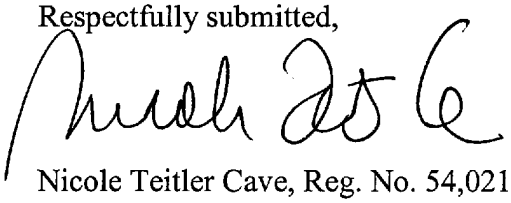

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